IT110-Computer Organizations

Assignment-3 solutions 5 marks

Question1

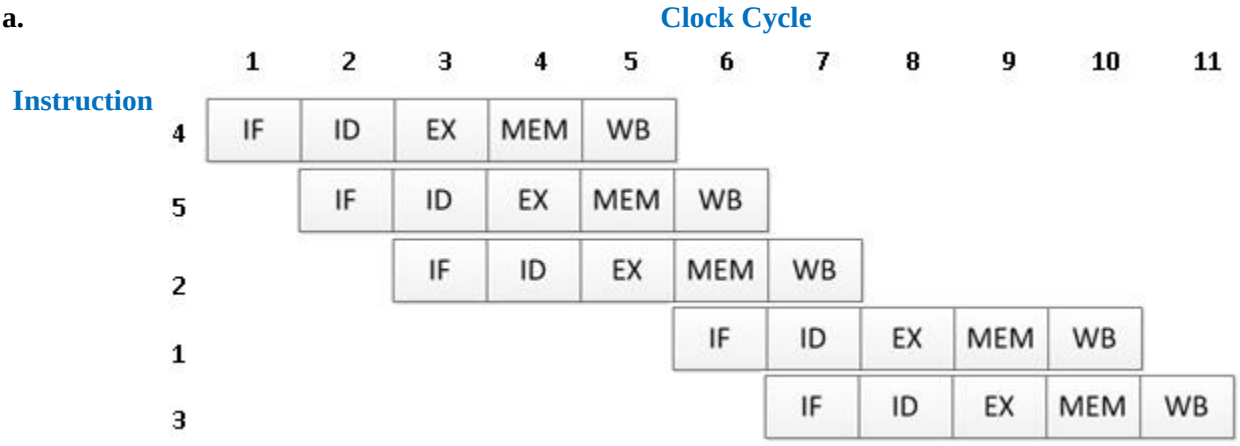
a. Execute all five instructions by using ***pipelining***.
b. What is the ***minimum*** number of clock cycles that will be required to execute all instructions?

Suppose the CPU has to execute 5 instructions. For each instruction, there are 5 stages of execution (given below) and each stage takes one clock cycle to complete.

Instruction 1 is dependent on instruction 4, instruction 3 is dependent on instruction 5 whereas instruction 2 is independent.

Solution:

a.



b. At minimum, 11 clocks are required to complete the given 5 instructions.

Question2:

Execute the following instruction by using:
0 address machine, 1 address machine, 2 address machine, 2 address machine using registers, 3 address machine and 3 address machine with registers.

$$A = a + c - b * e * f + w$$

Solution:

- 0 address machine

CODE	Memory Refrances
PUSH a	1
PUSH c	1
ADD	0
PUSH b	1
PUSH e	1
PUSH f	1
MUL	0
SUB	0
PUSH w	1
ADD	0
POP A	1

- 1 address machine

CODE	Memory Refrances
LOAD a	1
ADD C	1
STORE T1	1
LOAD B	1
MUL e	1
MUL f	1
STORE T2	1
LOAD T1	1
SUB T2	1
ADD w	1
STORE A	1

- 2 address machine

CODE	Memory Refrances
MOVE T1 , a	2
ADD T1 , c	3
MOVE T2 , b	2
MUL T2, e	3
MUL T2, f	3
SUB T1, T2	3
ADD T1 , w	3
MOVE A , T1	2

- 2 address machine using registers (1 ½ address machine)

CODE	Memory Refrances
MOVE R1 , a	1
ADD R1 , c	1
MOVE R2 , b	1
MUL R2, e	1
MUL R2, f	1
SUB R1, R2	0
ADD R1 , w	1
MOVE A , R1	1

- 3 address machine

CODE	Memory Refrances
ADD T1 , a , c	3
MUL T2 , b , e	3
MUL T2 , T2, , f	3
SUB T1 , T1 , T2	3
ADD A , T1 , w	3

- 3 address machine using registers

CODE	Memory Refrances
ADD R1 , a , c	2
MUL R2 , b , e	2
MUL R2 , R2, , f	1
SUB R1 , R1 , R2	0
ADD A , R1 , w	2

Question 3:

Define the characteristics of RISC?

Answer: RISC (Reduced Instruction Set Computers)

- Lower number of operations
- Compilers have more work to do
- Small no of instruction formats
- All instructions take one cycle
- Load or store architecture
- Smaller no of transistors, lower cpu complexity, therefore lower cpu prices.