RISC and CISC architectures.

CISC: Complex Instruction Set Architecture. It is an approach that attempts to minimize the number of instructions per program, sacrificing the number of cycles per instruction.

General characteristics:

- **High number of operations (300+)**
- **Compilers have less work to do to translate HLL into machine code.**
- **Large number of instruction formats**
- **Multi-clock cycle instructions**
- **Fewer registers; more memory access**
- **Large number of transistors, CPU complexity, therefore higher CPU prices**

Number of register:

- From 2 to 16 register

Instruction Set Architecture:

- **IBM System/360: a mainframe computer system family announced by IBM. It was the first family of computers designed to cover the complete range of applications, from small to large, both commercial and scientific.**
- **VAX: an instruction set architecture developed by Digital Equipment Corporation (DEC) in the mid-1970s.**
- **PDP-11: a series of 16-bit minicomputers sold by Digital Equipment Corporation (DEC) from 1970 into the 1990s, one of a succession of products in the PDP series.**

RISC: Reduced Instruction Set Architecture is the opposite, reducing the cycles per instruction at the cost of the number of instructions per program

General characteristics:

- **Lower number of operations (150+)**
- **Compilers have more work to do.**
- **Small number of instruction formats**
- **All instructions take one cycle.**
- **Load/store architecture**
- **Smaller number of transistors, lower CPU complexity, therefore lower CPU prices**

Number of register:

- **General purpose registers: 32 general purpose registers**
- **32 floating point registers**

RISC and CISC architectures.

Instruction Set Architecture:

- Load/store architecture (also called register-register or RR architecture) which fetches operands and results indirectly from main memory through a lot of scalar registers. Other architecture is storage-storage or SS in which source operands and final results are retrieved directly from memory.

CISC and RISC Architectures Comparison:

CISC	RISC
Focus on hardware	Focus on software
Includes multi-clock complex instructions	Single-clock, reduced instruction only
Memory-to-memory: "LOAD" and "STORE" incorporated in instructions	Register to register: "LOAD" and "STORE" are independent instructions
Small code sizes, high cycles per second	Low cycles per second, large code sizes
Transistors used for storing complex instructions	Spends more transistors on memory registers

References: Slides, Site No.1 , Site No.2 , Site No.3 , Site No.4